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Unit I**Chapter 1 : Digital Logic Families 1-1 to 1-36**

Syllabus : Classification and characteristics of digital logic families : Speed, Power dissipation, Figure of merit, Fan in, Fan out, Current, Voltage, Noise immunity, Operating temperatures and power supply requirements. TTL logic, Operation of TTL NAND gate, Active pull up, Wired AND, Open collector output, Unconnected inputs. Tri-state logic, CMOS logic : CMOS inverter, NAND, NOR gates, Unconnected inputs, Wired logic, Open drain output, Interfacing CMOS and TTL, Data sheet specifications.

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Unit II

Chapter 2 : Combinational Logic Design 2-1 to 2-40

Syllabus : Definition of combinational logic, Canonical forms, Standard representations for logic functions, K-map representation of logic functions (SOP and POS forms), Minimization of logical functions for minterms and maxterms (upto 4 variables), Don't care conditions, Introduction to Quine Mc-Cluskey method, Quine McCluskey using don't care terms, Reduced prime implicants tables.

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Units II & III

Chapter 3 : Combinational Circuits 3-1 to 3-60

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Unit IV

Chapter 4 : Flip Flops	4-1 to 4-42
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Syllabus : 1 bit memory cell, Clocked SR, JK, MS JK flip flop, D and T flipflops, Use of preset and clear terminals, Hold and setup time and metastability, Excitation table for flipflops, Conversion of flipflops, Typical data sheet specifications of Flip flop, Applications of flip flops, Clock skew, Clock jitter, Effect on synchronous design.

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