

**Article-A : Pre-requisites A-1 to A-04**

A.1	Binary Addition	A-2
A.1.1	Sum and Carry	A-2
A.2	Binary Subtraction	A-2
A.2.1	Subtraction and Borrow	A-2
A.3	1's Complement of a Binary Number	A-2
A.4	2's Complement	A-3
A.5	Binary Coded Decimal (BCD) Code	A-3
A.6	Non - weighted Codes	A-3
A.6.1	Excess - 3 Code	A-4
A.7	Gray Code	A-4

Unit I**Chapter 1 : Digital Logic Families 1-1 to 1-36**

Syllabus : Classification and characteristics of digital logic families : Speed, Power dissipation, Figure of merit, Fan in, Fan out, Current, Voltage, Noise immunity, Operating temperatures and power supply requirements. TTL logic, Operation of TTL NAND gate, Active pull up, Wired AND, Open collector output, Unconnected inputs. Tri-state logic, CMOS logic : CMOS inverter, NAND, NOR gates, Unconnected inputs, Wired logic, Open drain output, Interfacing CMOS and TTL, Data sheet specifications.

1.1	Introduction	1-2
1.2	Classification of Logic Families	1-2
1.2.1	Classification Based on Devices Used ...	1-2
1.3	Characteristics of Digital ICs	1-3
1.3.1	Voltage and Current Parameters	1-3
1.3.2	Fan-in and Fan-out	1-4
1.3.3	Noise Margin	1-5
1.3.4	Propagation Delay	1-5
1.3.5	Power Dissipation	1-6
1.3.6	Operating Temperature	1-6
1.3.7	Figure of Merit (Speed Power Product (SPP))	1-6
1.3.8	Invalid Voltage Levels	1-7
1.3.9	Current Sourcing and Current Sinking ...	1-7
1.3.10	Power Supply Requirements	1-7
1.4	Transistor-Transistor Logic (TTL)	1-8
1.4.1	The Multiple Emitter Transistor	1-8
1.4.2	Two Input TTL-NAND Gate (Totem-pole Output)	1-8
1.4.3	Totem-pole (Active Pull up) Output Stage	1-10
1.4.4	Unconnected Inputs	1-11
1.4.5	Clamping Diodes	1-12
1.4.6	5400 Series	1-12

1.5	Sourcing and Sinking in TTL	1-12
1.5.1	Current Sinking Action	1-12
1.5.2	Current Sourcing Action	1-13
1.6	Wired AND Connection (TTL)	1-13
1.7	Open Collector Outputs (TTL)	1-14
1.7.1	Disadvantages of Open Collector Output	1-15
1.7.2	Advantage of Open Collector Output ...	1-15
1.7.3	Wired ANDing	1-15
1.7.4	Comparison of Totem-pole and Open Collector Outputs	1-16
1.8	Tristate (Three state) TTL Devices	1-17
1.8.1	Advantages of Tristate	1-18
1.8.2	Tristate Buffers	1-18
1.8.3	Applications of Tristate Buffers (Bus Organization)	1-18
1.8.4	A TRI-STATE Inverter	1-18
1.9	Standard TTL Characteristics	1-19
1.10	Advantages and Disadvantages of TTL	1-20
1.10.1	Advantages of TTL	1-20
1.10.2	Disadvantages of TTL	1-20
1.11	MOS - Logic Family	1-21
1.12	CMOS Logic	1-21
1.12.1	CMOS Inverter	1-21
1.12.2	CMOS NOR Gate	1-22
1.12.3	CMOS NAND Gate	1-23
1.12.4	CMOS Series	1-24
1.13	CMOS Characteristics	1-25
1.13.1	Power Supply Voltage	1-25
1.13.2	Logic Voltage Levels	1-25
1.13.3	Noise Margins	1-25
1.13.4	Power Dissipation	1-25
1.13.5	Fan Out	1-26
1.13.6	Switching Speed	1-26
1.13.7	Unconnected Inputs	1-26
1.14	Advantages and Disadvantages of CMOS	1-27
1.14.1	Advantages of CMOS	1-27
1.14.2	Disadvantages of CMOS	1-27
1.15	Interfacing	1-27
1.15.1	TTL to CMOS Interfacing	1-27
1.15.2	TTL Driving High Voltage CMOS	1-28
1.15.3	Interfacing using Level-Shifter (TTL to High Voltage CMOS)	1-28
1.15.4	CMOS to TTL Interface	1-29
1.15.5	CMOS Driving TTL in the HIGH State	1-29



1.15.6	CMOS Driving TTL in the LOW State ...	1-30
1.15.7	High Voltage CMOS Driving TTL	1-30
1.16	Comparison of CMOS and TTL	1-30
1.17	7400 TTL Quad 2-input NAND Gate.....	1-31
1.18	4011B Quad 2-input CMOS NAND Gate.....	1-33
•	Review Questions	1-36

Unit II

Chapter 2 : Combinational Logic Design 2-1 to 2-40

Syllabus : Definition of combinational logic, Canonical forms, Standard representations for logic functions, K-map representation of logic functions (SOP and POS forms), Minimization of logical functions for minterms and maxterms (upto 4 variables), Don't care conditions, Introduction to Quine Mc-Cluskey method, Quine McCluskey using don't care terms, Reduced prime implicants tables.

2.1	Binary Logic and Logic Levels	2-2
2.2	Introduction of Boolean Algebra	2-2
2.2.1	Logic Gates	2-2
2.2.2	Gates, Symbols and Boolean Expression	2-2
2.2.3	An Overview of Boolean (Binary) Algebra	2-3
2.2.4	Boolean Laws	2-3
2.2.5	De-Morgan's Theorems	2-4
2.3	System or Circuit	2-5
2.3.1	Digital Systems	2-5
2.3.2	Types of Digital Systems	2-6
2.3.3	Combinational Circuit Design	2-6
2.4	Standard Representations for Logical Functions	2-7
2.4.1	Sum-of-Products (SOP) Form	2-7
2.4.2	Product of the Sums Form (POS)	2-7
2.4.3	Standard or Canonical SOP and POS Forms	2-8
2.4.4	Conversion of a Logic Expression to Standard SOP or POS Form	2-8
2.5	Concepts of Minterm and Maxterm	2-9
2.5.1	Representation of Logical Expressions using Minterms and Maxterms	2-10
2.5.2	Writing SOP and POS Forms for a Given Truth Table	2-10
2.5.3	Representation of Truth Table using Standard SOP Expression	2-10
2.5.4	To Write a Standard POS Expression for a Given Truth Table	2-11

2.5.5	Conversion from SOP to POS and Vice Versa	2-11
2.6	Methods to Simplify the Boolean Functions	2-13
2.6.1	Algebraic Simplification	2-13
2.6.2	Disadvantages of Algebraic Method of Simplification	2-14
2.7	Karnaugh-Map Simplification	2-14
2.7.1	K-map Structure	2-14
2.7.2	K-map Boxes and Associated Product Terms	2-15
2.7.3	Alternative Way to Label the K-map	2-16
2.7.4	Truth Table to K-map	2-16
2.7.5	Representation of Standard SOP Form on K-map	2-17
2.8	Minimization of Boolean Expressions using K-map	2-17
2.8.1	How does Simplification Takes Place ?	2-18
2.8.2	Way of Grouping (Pairs, Quads and Octets)	2-18
2.8.3	Grouping Two Adjacent One's (Pairs) ..	2-18
2.8.4	Grouping Four Adjacent Ones (Quad) ..	2-19
2.8.5	Grouping Eight Adjacent Ones (Octet) ..	2-20
2.9	Minimization of SOP Expressions (K Map Simplification)	2-21
2.9.1	Elimination of a Redundant Group	2-23
2.9.2	Minimization of Logic Functions not Specified in Standard SOP Form	2-25
2.9.3	Don't Care Conditions	2-26
2.9.3	Disadvantages of K-map Technique	2-28
2.10	Product of Sum (POS) Simplification	2-28
2.10.1	K-map Representation of POS Form ...	2-28
2.10.2	Representation of Standard POS form on K-map	2-29
2.10.3	Simplification of Standard POS Form using K-map	2-30
2.11	Quine Mc-Cluskey Minimization Technique (Tabular Method)	2-32
2.11.1	Important Definitions	2-33
•	Review Questions	2-39

Units II & III

Chapter 3 : Combinational Circuits 3-1 to 3-60

Syllabus : Design examples : Arithmetic circuits, BCD - to - 7 segment decoder, Code converters, Adders and their use as subtractors, Look ahead carry, ALU, Digital comparator, Parity generators / checkers, Multiplexers and their use in combinational logic designs, Multiplexer trees, Demultiplexers and their use in combinational logic designs, Decoders, Demultiplexer trees.



3.1	Analysis and Design of Combinational Circuits	3-2	3.11.1	Necessity of Multiplexers	3-30
3.1.1	Analysis of a Combinational Circuit	3-2	3.11.2	Advantages of Multiplexers	3-30
3.1.2	Design of Combinational Logic using Statements	3-2	3.12	Types of Multiplexers	3-30
3.2	Design Examples	3-5	3.12.1	2 : 1 Multiplexer	3-30
3.3	Binary Adders and Subtractors	3-5	3.12.2	A 4 : 1 Multiplexer	3-30
3.3.1	Types of Binary Adders	3-5	3.12.3	8 : 1 Multiplexer	3-31
3.3.2	Half Adder	3-5	3.12.4	Applications of a Multiplexer	3-32
3.3.3	Full Adder	3-7	3.13	Multiplexer Tree / Cascading of Multiplexer	3-32
3.3.4	Full Adder using Half Adder	3-8	3.14	Use of Multiplexers in Combinational Logic Design	3-34
3.3.5	Applications of Full Adder	3-8	3.14.1	Implementation of a Logical Expression in the Standard SOP Form	3-34
3.3.6	Binary Subtractors	3-8	3.14.2	Implementation of a Logical Expression in the Non-standard Form	3-40
3.3.7	Half Subtractor	3-8	3.14.3	Implementing a Standard POS Expression using Multiplexer	3-40
3.3.8	Full Subtractor	3-9	3.14.4	Implementation of Boolean Expression with Don't Care Conditions	3-42
3.3.9	Full Subtractor using Half Subtractors	3-10	3.15	Demultiplexers	3-42
3.4	BCD to Seven Segment Decoder (Common Anode Display)	3-11	3.15.1	Demultiplexer Principle	3-42
3.4.1	BCD to 7 Segment Decoder using a Common Cathode Display	3-12	3.16	Types of Demultiplexers	3-43
3.5	Code Converters	3-14	3.16.1	1 : 2 Demultiplexer	3-43
3.5.1	Excess - 3 to BCD Code Converter	3-14	3.16.2	1 : 4 Demultiplexer	3-44
3.5.2	Binary to Gray Code Converter	3-15	3.16.3	1 : 8 Demultiplexer	3-45
3.5.3	Gray to Binary Code Converter	3-16	3.17	Demultiplexer Tree	3-45
3.6	The n-Bit Parallel Adder	3-18	3.17.1	Comparison of Multiplexer and Demultiplexer	3-47
3.6.1	A Four Bit Parallel Adder Using Full Adders	3-18	3.17.2	Use of DEMUX in Combinational Logic Design	3-47
3.6.2	Propagation Delay in Parallel Adder	3-18	3.18	Encoders	3-49
3.6.3	Look Ahead – Carry Adder	3-19	3.18.1	Types of Encoders	3-49
3.6.4	Four Bit Fast Adder with Look-Ahead Carry	3-20	3.19	Priority Encoder	3-49
3.6.5	Fast Adder IC 74 LS 83 / 74 LS 283	3-20	3.20	Decoder	3-50
3.6.6	Four Bit Binary Adder using IC 7483	3-21	3.20.1	2 to 4 Line Decoder	3-50
3.7	n-bit Parallel Subtractor (Use of Adder as Subtractor)	3-21	3.20.2	Difference Between Decoder and Demultiplexer	3-51
3.7.1	4 Bit Parallel Subtractor using 2's Complement	3-21	3.20.3	Comparison of Multiplexer and Decoder	3-51
3.7.2	4-Bit Binary Parallel Adder/Subtractor	3-22	3.20.4	Demultiplexer as Decoder	3-52
3.8	BCD Adder	3-22	3.20.5	3 to 8 Line Decoder	3-52
3.8.1	Block Diagram of BCD Adder	3-22	3.20.6	1 : 8 DEMUX Operated as 3:8 Decoder	3-52
3.8.2	Design of Combinational Circuit	3-23	3.20.7	IC 74138 as 3 : 8 Decoder	3-53
3.9	Digital Comparators	3-24	3.20.8	4 Line to 16 Line Decoder using 3 : 8 Decoder	3-54
3.9.1	1-Bit Binary Comparator	3-24	3.20.9	Combinational Logic Design Using Decoders	3-54
3.9.2	A 2-Bit Comparator	3-25			
3.10	Arithmetic Logic Unit (ALU)	3-26			
3.10.1	Cascading of two 74181 ALUs	3-28			
3.11	Multiplexer (Data Selector)	3-29			



3.21	Parity Generators / Checkers	3-56
3.21.1	Parity Generator	3-56
3.21.2	Parity Checker	3-58
•	Review Questions	3-59

Unit IV

Chapter 4 : Flip Flops	4-1 to 4-42
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Syllabus : 1 bit memory cell, Clocked SR, JK, MS JK flip flop, D and T flipflops, Use of preset and clear terminals, Hold and setup time and metastability, Excitation table for flipflops, Conversion of flipflops, Typical data sheet specifications of Flip flop, Applications of flip flops, Clock skew, Clock jitter, Effect on synchronous design.

4.1	Introduction	4-2	4.7.2	Difference between Latch and Flip-flop	4-13
4.1.1	Combinational Circuits	4-2	4.8	Edge Triggered Flip Flops	4-14
4.1.2	Sequential Circuits	4-2	4.8.1	Types of Edge Triggered Flip Flops (Clocked FFs)	4-14
4.1.3	Clock Signal	4-2	4.8.2	Positive Edge Triggered S-R Flip Flop	4-14
4.1.4	Clock Skew	4-2	4.8.3	Negative Edge Triggered S-R Flip Flop	4-15
4.1.5	Comparison of Combinational and Sequential Circuits	4-3	4.9	Edge Triggered D Flip Flop	4-16
4.1.6	1-Bit Memory Cell (Basic Bistable Element)	4-3	4.9.1	Positive Edge Triggered D Flip Flop	4-16
4.1.7	Latch	4-4	4.9.2	Negative Edge Triggered D Flip Flop ...	4-17
4.2	S-R Latch using NOR Gates	4-4	4.10	Edge Triggered J-K Flip Flop	4-17
4.2.1	Operation of S-R Latch	4-5	4.10.1	Positive Edge Triggered JK Flip Flop ...	4-17
4.2.2	Symbol and Truth Table of S-R Latch	4-6	4.10.2	Characteristic Equation of JK Flip Flop	4-19
4.2.3	Characteristic Equation	4-6	4.10.3	How does an Edge Triggered JK FF Avoid Race Around Condition ?	4-19
4.2.4	NAND Latch [S-R Latch using NAND Gates]	4-6	4.10.4	Negative Edge Triggered JK flip-flop ...	4-19
4.3	Triggering Methods	4-8	4.11	Toggle Flip Flop (T Flip Flop)	4-20
4.3.1	Concept of Level Triggering	4-8	4.11.1	Positive Edge Triggered T-FF	4-20
4.3.2	Types of Level Triggered Flip-flops	4-8	4.11.2	Negative Edge Triggered T Flip Flop ...	4-21
4.3.3	Concept of Edge Triggering	4-8	4.11.3	Application of T F/F	4-21
4.3.4	Types of Edge Triggered Flip Flops	4-9	4.12	Master Slave (MS) JK Flip Flop	4-21
4.4	Gated Latches (Level Triggered SR Flip Flop)	4-9	4.13	Preset and Clear Inputs	4-23
4.4.1	Types of Level Triggered (Clocked) Flip Flops	4-9	4.13.1	S-R Flip-Flop with Preset and Clear Inputs	4-23
4.5	The Gated S-R Latch (Clocked S-R Flip Flop)	4-9	4.13.2	Synchronous Preset and Clear Inputs	4-24
4.5.1	Positive Level Triggered SR Flip-flop	4-9	4.13.3	JK Flip Flop with Preset and Clear Inputs	4-24
4.5.2	Negative Level Triggered SR Flip Flop	4-10	4.13.4	Applications of JK Flip Flop	4-25
4.5.3	Disadvantage of S-R Latch	4-11	4.14	Various Representations of Flip Flops	4-25
4.5.4	Application of S-R Latch	4-11	4.14.1	Characteristic Equations	4-25
4.6	The Gated D Latch (Clocked D Flip Flop)	4-11	4.15	Excitation Table of Flip-Flop	4-25
4.7	Gated JK Latch (Level Triggered JK Flip Flop)	4-12	4.15.1	Excitation Table of SR Flip Flops	4-25
4.7.1	Race Around Condition in JK Latch	4-13	4.15.2	Excitation Table of D Flip Flop	4-26
			4.15.3	Excitation Table of JK Flip Flop	4-26
			4.15.4	Excitation Table of T Flip Flop	4-26
			4.16	Conversion of Flip Flops	4-26
			4.16.1	Conversion from S-R Flip Flop to D Flip Flop	4-27
			4.16.2	Conversion of JK FF to T FF	4-27
			4.16.3	SR Flip Flop to T Flip Flop	4-28
			4.16.4	SR Flip Flop to JK Flip Flop	4-28
			4.16.5	Conversion of D Flip Flop to T Flip Flop	4-29



4.16.6	T Flip Flop to D Flip Flop Conversion	4-29
4.16.7	JK Flip Flop to D Flip Flop Conversion	4-30
4.16.8	JK Flip Flop to SR Flip Flop Conversion	4-30
4.16.9	D FF to SR FF Conversion	4-31
4.16.10	T FF to SR FF Conversion	4-31
4.16.11	Conversion from D FF to JK FF	4-31
4.17	Flip Flop Timing Considerations	4-32
4.17.1	Set Up and Hold Times	4-32
4.17.2	Propagation Delays	4-33
4.17.3	Maximum Clocking Frequency f_{max}	4-33
4.18	Flip Flop Metastability	4-33
4.18.1	Characteristics, Causes and Effects of Metastability	4-34
4.18.2	Illustration of Metastability	4-34
4.19	Applications of Flip Flops	4-35
4.20	Analysis of Clocked Sequential Circuits	4-35
4.20.1	State Table	4-35
4.20.2	State Diagram	4-35
4.20.3	State Equation	4-36
4.21	Design of Clocked Synchronous State Machine using State Diagram	4-38
4.22	Clock Jitter and it's Effects on Synchronous Design	4-39
4.23	Typical Data Sheet Specifications of Flip flop	4-40
4.23.1	SN74LS74A : Dual D-Type Positive Edge-triggered Flip-Flop Low Power Schottky	4-40
4.23.2	SN74LS76A : Dual JK Flip-Flop with Set and Clear Low Power Schottky	4-41
	• Review Questions	4-42

Unit IV

Chapter 5 : Registers 5-1 to 5-20

Syllabus : Registers, Shift registers, Counters (Ring counters, Twisted ring counters).

5.1	Introduction	5-2
5.2	Data Formats	5-2
5.3	Classification of Registers	5-2
5.4	Buffer Registers	5-2
5.5	Shift Registers	5-3
5.5.1	Serial Input Serial Output (Shift Left Mode)	5-4

5.5.2	Serial In Serial Out (Shift Right Mode)	5-5
5.5.3	Applications of Serial Operation	5-6
5.6	Serial In Parallel Out (SIPO)	5-7
5.7	Parallel In Serial Out Mode (PISO)	5-8
5.8	Parallel In Parallel Out (PIPO)	5-9
5.9	Bidirectional Shift Register	5-9
5.9.1	A 3-bit Bidirectional Register using the JK Flip Flops	5-10
5.10	Universal Shift Register	5-10
5.10.1	Universal Shift Register using Multiplexers and D-flip flops	5-11
5.11	Applications of Shift Registers	5-12
5.11.1	Serial to Parallel Converter	5-12
5.11.2	Parallel to Serial Converter	5-12
5.12	Ring Counter	5-12
5.13	Johnson's Counter (Twisted / Switch Tail Ring Counter)	5-14
5.13.1	Johnson's Counter using D Flip-flops	5-15
5.14	Sequence Generator	5-15
5.14.1	Sequence Generator using Shift Register	5-15
	• Review Questions	5-19

Unit IV

Chapter 6 : Counters 6-1 to 6-40

Syllabus : Ripple counters, MOD-N counters, Up/down counters, Synchronous counters, Lock out, Sequence generators.

6.1	Introduction	6-2
6.1.1	Types of Counters	6-2
6.1.2	Classification of Counters	6-2
6.2	2-Bit Asynchronous / Ripple Up Counters	6-2
6.2.1	Two Bit Asynchronous Up Counter using JK Flip-Flops	6-4
6.2.2	3 Bit Asynchronous Up Counter	6-4
6.2.3	4 Bit Asynchronous up Counter	6-5
6.2.4	State Diagram of a Counter	6-6
6.3	Asynchronous Down Counters	6-6
6.3.1	3- Bit Asynchronous Down Counter	6-6
6.4	UP / DOWN Counters	6-7
6.4.1	UP/DOWN Ripple Counters	6-8
6.4.2	3-bit Up Down Ripple Counters	6-8
6.5	Modulus of the Counter (MOD-N Counter)	6-10
6.5.1	Design of Asynchronous MOD Counters	6-10



6.5.2	Frequency Division Taking Place in Asynchronous Counters	6-13
6.5.3	Decade (BCD) Ripple Counter	6-14
6.6	Problems Faced by Ripple Counters	6-15
6.6.1	Glitch	6-15
6.6.2	Disadvantages of Ripple Counters	6-16
6.7	Synchronous Counters	6-16
6.7.1	2-Bit Synchronous up Counter	6-16
6.7.2	3-Bit Synchronous Binary up Counter	6-17
6.7.3	Design of the 3 Bit Synchronous Counter.....	6-18
6.7.4	Four Bit Synchronous Up Counter	6-20
6.8	Modulo – N Synchronous Counters	6-20
6.8.1	Synchronous Decade Counter	6-20
6.9	UP / DOWN Synchronous Counter	6-27
6.9.1	3-bit Up/Down Synchronous Counter ...	6-27
6.9.2	Advantages of Synchronous Counter ...	6-28
6.9.3	Comparison of Synchronous and Asynchronous Counters	6-28
6.10	Lock Out Condition	6-28
6.10.1	Bushless Circuit	6-29
6.11	Bush Diagram	6-32
6.12	Applications of Counters	6-34
6.12.1	Comparison of Counters and Registers	6-34
6.13	Sequence Generator	6-34
6.13.1	Sequence Generator using Counters ...	6-34
	• Review Questions	6-39

Unit V

Chapter 7 : State Machines 7-1 to 7-28

Syllabus : Basic design steps - State diagram, State table, State reduction, State assignment, Mealy and Moore machines representation, Implementation, Finite state machine implementation, Sequence detector.

7.1	General Model of Sequential Circuits	7-2
7.1.1	Classification of Sequential Circuits	7-2
7.2	Models for Synchronous Sequential Circuits	7-2
7.3	Moore Circuit	7-3
7.3.1	Example of Moore Circuit	7-3
7.4	Mealy Circuit	7-4
7.4.1	Example of Mealy Circuit	7-4
7.4.2	Comparison of Moore and Mealy Models	7-5
7.4.3	State Diagram of a Moore Circuit	7-5
7.5	Finite State Machine (FSM)	7-5
7.5.1	Advantages of FSM	7-6

7.5.2	Disadvantages of FSM	7-6
7.5.3	State Machine Notations	7-6
7.5.4	Present States, Next State	7-6
7.6	Analysis of Clocked Sequential Circuits	7-6
7.7	Design Procedure for Clocked Sequential Circuits	7-10
7.8	State Reduction and Assignments	7-10
7.8.1	Row Elimination Method	7-11
7.8.2	Example on Row Elimination Method....	7-11
7.9	State Assignment	7-12
7.10	Design of Clocked Synchronous State Machine using State Diagram	7-15
7.11	Design using Unused States	7-17
7.11.1	Synthesis Table	7-17
7.12	Sequence Detector	7-20
	• Review Questions	7-27

Unit V

Chapter 8 : Algorithmic State Machines 8-1 to 8-22

Syllabus : Introduction to algorithmic state machines - Construction of ASM chart and realization for sequential circuits.

8.1	Introduction to ASM (FSM and ASM)	8-2
8.2	ASM Chart Notations	8-2
8.2.1	The State Box	8-2
8.2.2	Decision Box	8-2
8.2.3	Conditional Box	8-3
8.2.4	ASM Block	8-3
8.3	How to use the ASM Chart for Sequential Circuit Design ?	8-6
8.3.1	Realization of the Logic Circuit	8-7
8.3.2	Design with Multiplexers	8-11
	• Review Questions	8-22

Unit VI

Chapter 9 : Programmable Logic Devices 9-1 to 9-26

Syllabus : Programmable logic devices : Detail architecture, Study of PROM, PAL, PLA, General architecture, Features and typical specifications of FPGA and CPLD, Designing combinational circuits using PLDs.

9.1	Introduction to PLDs	9-2
9.1.1	Advantages of PLDs	9-2
9.1.2	Types of PLDs	9-2
9.2	ROM used as PLD	9-3



9.2.1	Types of ROMs	9-3	10.4.2	Random Access Memory (RWM or RAM)	10-5
9.2.2	Internal Logic of a ROM	9-3	10.4.3	Read Only Memories (ROM)	10-5
9.2.3	Implementation of a Combinational Circuit (Generating the Boolean Function)	9-5	10.4.4	Content Accessible Memories (CAM)	10-6
9.2.4	Advantages of ROM as PLD	9-7	10.5	Classification Based on Physical Characteristics	10-6
9.2.5	Disadvantages of ROM as PLD	9-7	10.5.1	Erasable or Non-erasable Memories ...	10-7
9.3	Programmable Logic Array (PLA)	9-7	10.5.2	Ultraviolet Erasable Programmable ROM (EPROM)	10-7
9.3.1	The Programming Procedure for PLA	9-9	10.5.3	Volatile or Non-volatile Memories	10-7
9.3.2	Expansion of PLA Capacity	9-9	10.6	Classification Based on Mode of Access	10-8
9.3.3	Application Areas of PLA	9-9	10.6.1	Sequential Access	10-8
9.3.4	Designing of Combinational Circuit using PLA	9-9	10.6.2	Random Access	10-8
9.3.5	How to Specify the Size of a PLA ?	9-10	10.7	Classification Based on Fabrication Technology	10-8
9.4	Programmable Array Logic (PAL)	9-17	10.8	Internal Organization of Memory	10-8
9.4.1	Solved Examples on PAL	9-19	10.8.1	Write Operation	10-9
9.4.2	Types of PAL Devices	9-22	10.8.2	Timing Characteristics of the Write Cycle	10-9
9.4.3	Registered PALs	9-22	10.8.3	Read Operation	10-10
9.4.4	Configurable PAL	9-22	10.8.4	Timing Characteristics of Read Cycle	10-10
9.5	Generic Array Logic Devices (GAL)	9-22	10.9	Expanding Memory Size	10-11
9.5.1	Comparison of PROM, PLA and PAL ...	9-22	10.9.1	Expanding the Word Size	10-12
9.6	Complex Programmable Logic Devices (CPLDs)	9-23	10.9.2	Expanding Word Capacity	10-12
9.7	Field Programmable Gate Array (FPGA)	9-24	10.10	Read Only Memory (ROM)	10-16
9.7.1	Comparison of CPLD and FPGA	9-25	10.10.1	Application of ROM	10-16
9.8	Characteristics of Various PLDs	9-25	10.10.2	ROM Manufacturing	10-17
	• Review Questions	9-26	10.10.3	ROM Organization	10-17
Unit VI					
Chapter 10 : Semiconductor Memories 10-1 to 10-26					
Syllabus : Semiconductor memories : Memory organization and operation, Expanding memory size, Classification and characteristics of memories, RAM, ROM, EPROM, EEPROM, NVRAM, SRAM and DRAM.					
10.1	Introduction	10-2	10.11	Random Access Memory (RAM)	10-18
10.1.1	Advantages of Semiconductor Memory	10-2	10.12	Static RAM (SRAM)	10-19
10.2	Memory Organization and Operation	10-2	10.12.1	TTL RAM Cell	10-19
10.2.1	Memory Size	10-2	10.12.2	MOS Static RAM Cell	10-19
10.2.2	Block Diagram of a Memory Device	10-2	10.12.3	Dynamic RAM (DRAM)	10-20
10.3	Classification and Characteristics of Memories ..	10-4	10.12.4	Dynamic MOS RAM Cell	10-21
10.3.1	Important Characteristics of Memory	10-4	10.12.5	Comparison of SRAM and DRAM	10-22
10.4	Classification Based on Principle of Operation	10-4	10.12.6	Comparison of RAM and ROM	10-22
10.4.1	Sequential Memories	10-4	10.13	EEPROM (E ² PROM)	10-22
			10.13.1	Comparison of EPROM and EEPROM	10-23
			10.14	NVRAM	10-23
				• Review Questions	10-23